Amendments to the Claims:

1. (currently amended) A circuit for demodulating at least one modulated signal such as a measuring signal of a sensor, comprising

at least one input to which the modulated signal may be applied, and

at least one switched-capacitor network connected to the input for demodulating the signal, the switched-capacitor network including at least two inputs and at least one switched-capacitor amplifier and at least one switched-capacitor integrator, wherein the at least one switched-capacitor amplifier comprises a positive delayed switched-capacitor amplifier, which multiplies two input signals each by at least one factor.

2.-4. (cancelled)

5. (currently amended) The circuit of claim 1 [[4]], wherein the network includes a second switched-capacitor amplifier which ~~(7)~~ comprises a positive delayed switched-capacitor amplifier, which ~~and/or~~ delays the applied input signal by a half cycle of a clock frequency, and ~~and/or~~ has an amplification of one.

6. (currently amended) The circuit of claim 5, wherein the network includes a third switched-capacitor amplifier which ~~(9)~~ comprises a positive delayed switched-capacitor amplifier, which ~~and/or~~ delays the applied input signal unamplified by a half cycle of the clock frequency.

7. (currently amended) The circuit of claim 6, wherein the network includes a fourth switched-capacitor amplifier which ~~(10)~~ comprises a positive delayed switched-capacitor amplifier, which ~~and/or~~ delays the applied input signal unamplified by a half cycle of the clock frequency.

8. (currently amended) The circuit of claim 7, wherein the network includes a fifth switched-capacitor amplifier which ~~(11)~~ comprises a positive delayed switched-capacitor amplifier, which ~~and/or~~ delays the applied input signal unamplified by a half cycle of the clock frequency.

9. (currently amended) The circuit of claim 1 [[2]], wherein the output of the one ~~a first~~ switched-capacitor amplifier ~~(5)~~ is applied to an input of the one switched-capacitor integrator ~~(6, 8)~~.

10. (currently amended) The circuit of claim 9, wherein the output of the one switched-capacitor integrator ~~(6, 8)~~ is applied to a second input of the one ~~first~~ switched-capacitor amplifier ~~(5)~~.

11. (currently amended) The circuit of claim 6 wherein the output of the second switched-capacitor amplifier ~~(7)~~ is applied to an input of the third switched-capacitor amplifier ~~(9)~~.

12. (currently amended) The circuit of claim 7, wherein the output of the third switched-capacitor amplifier ~~(9)~~ is applied to an input of the fourth switched-capacitor amplifier ~~(10)~~.

13. (currently amended) The circuit of claim 8, wherein the output of the fourth switched-capacitor amplifier ~~(10)~~ is applied to an input of the fifth switched-capacitor amplifier ~~(11)~~.

14. (currently amended) The circuit of claim 8, wherein the output of the fifth switched-capacitor amplifier ~~(11)~~ is applied to a second input of the switched-capacitor integrator ~~(6, 8)~~.

15. (currently amended) The circuit of claim 14, wherein the at least one modulated signal is applied to a third input of the switched-capacitor integrator ~~(6, 8)~~.

16. (currently amended) The circuit of claim 14 wherein the switched-capacitor integrator ~~(8)~~ includes at least two integrator capacitances.

17. (currently amended) The circuit of claim 16, wherein the two integrator capacitances are used[[,]] for storing a previous signal and ~~and/or~~ computing a ~~the~~ reflected voltage wave.

18. (currently amended) The circuit of claim 1 [[2]], wherein the switched-capacitor network comprises a filter arrangement.

19. (currently amended) The circuit of claim 18, wherein the filter arrangement comprises an n-path lag wave filter that is formed by the at least one of the switched-capacitor amplifier ~~amplifiers (5, 7, 9, 10, 11) and/or~~ and the at least one switched-capacitor integrator ~~(6, 8)~~.

20. (original) The circuit of claim 18 wherein the coefficients of the filter arrangement are digitally programmable by means of at least one switch.

21. (original) The circuit of one of claim 1 further comprising a further switched-capacitor network whereby the demodulated signal of positive and negative values of a carrier frequency can be added.

22. (currently amended) A method of demodulating a modulated measuring signal of a sensor comprising the steps of

applying the signal to an input of a switched-capacitor network and operating the network so as to demodulate the signal, and

adding positive and negative values of a carrier frequency of the demodulated signal by means of a further switched-capacitor network.

23. (original) The method of claim 22, wherein the signal is filtered by means of a filter arrangement.

24. (original) The method of claim 22, wherein the signal is converted to a square-wave signal.

25. (original) The method of claim 22, wherein the signal is sampled at least once.

26. (cancelled)